Dini Group Turns to Tektronix Certus to Tackle Daunting FPGA Prototype Challenges

Customer Solution Summary

October 2012

Challenge

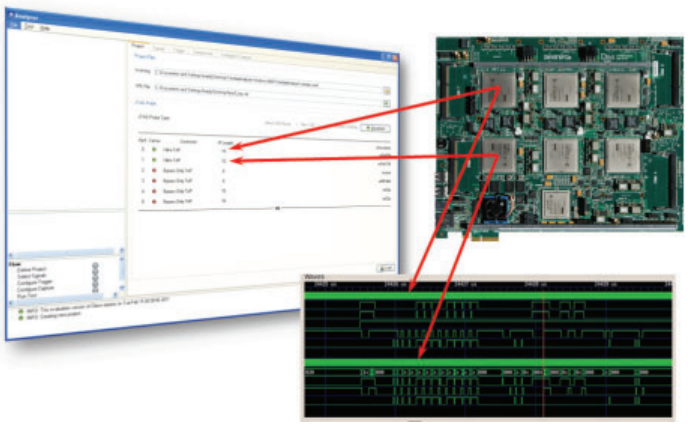
The debug of ASIC prototypes is a major productivity bottleneck for Dini Group and its customers. Due to long FPGA re-compile times, debug is a slow and painful process when using traditional tools.

Solution

Version 2.0 of the Tektronix Certus ASIC Prototyping Debug Solution has given Dini Group designers direct access to thousands of RTL-level signals in their FPGAs, reducing the need to re-compile for each new set of debug probes and changing the way they approach overall FPGA debug

Benefits

The Dini Group has realized significant time savings using Certus 2.0 primarily by reducing debug re-compile iterations. For one of their designs in the high-performance computing segment, each place and route iteration of the FPGA took more than three hours to complete. By using Certus 2.0 and speculatively instrumenting a large number of signals, Dini Group was able to reduce debug iterations from about 30 down to three, saving weeks of debug time on this one design alone.



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Big FPGA Boards

High Performance Computing

FPGA debug tools fall short for larger designs

Established in 1995 as a FPGA and ASIC consulting company, the Dini Group is now the market leader in FPGA-based ASIC prototyping hardware. Since its inception, the Dini Group has delivered more than ten billion ASIC gates worldwide to companies developing systems for the high-speed computing, telecommunications and cloud computing markets.

With the rise of the cloud and large-scale on-demand Web applications, Mike Dini, president of the Dini Group sees demand growing for custom high-speed ASIC processor prototypes involving anywhere from two to a dozen FPGAs. For these multi-FPGA prototypes, debugging has emerged as a major challenge. For both the Dini Group and its customers, the limitations of traditional FPGA debug tools represent a major productivity bottleneck.

While traditional FPGA debug tools can work for small designs with simple debug challenges, they fall short for larger designs.

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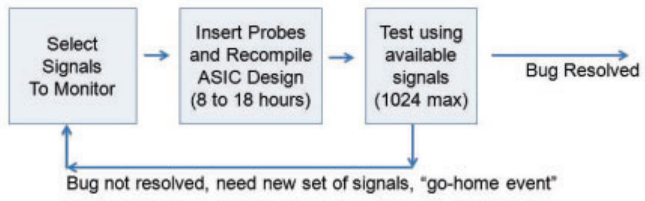
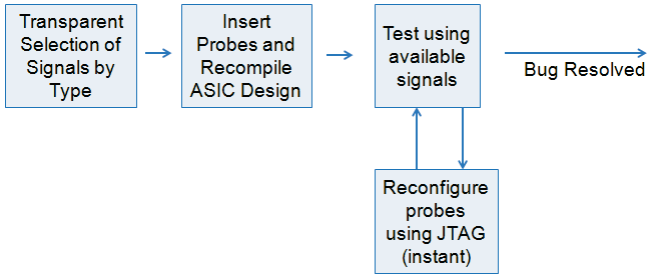


Debug Cycle with Traditional FPGA Debug Tools

With limited visibility, each debug iteration requires a recompile (8-18 hours), resulting in bug resolution on the order of weeks or months.



Debug Cycle with Certus-enabled Full RTL-level Visibility

The unique ability of the Certus debug platform from Tektronix to instrument unlimited signals and view any combination of these signals minimizes recompiles to completely streamline the debugging process. As a result, identifying, locating, and resolving bugs can be achieved in hours or days.

This is due to a number of inescapable realities associated with larger ASIC prototypes, including:

- The bugs are never where you think they are. When limited in the number of available signals, trying to select the right signals is nearly impossible during the first few attempts.
- For designs involving large FPGAs, gaining access to another set of signals requires 5-8 hours or more of processing time to generate a new FPGA programming file.
- Acquired IP blocks will have bugs and limited documentation, meaning the designer will need signal access to figure out how the IP works and to develop workarounds.
- Every design has multiple clock domains, multiple FPGAs or both. For efficient debug, these signals must be correlated across domains and chips for a system-wide view.

Certus, now on version 2.0, is the only debug tool in the industry to fully address these challenges, according to Neal Palmer, chief technology officer for the Dini Group.

"With Certus it's possible to capture as many signals as you want to capture. It all fits within an FPGA, it can go across multiple FPGAs, and you can have separate stations within multiple FPGAs all working together to capture your data. Until Certus, all these things were completely lacking within the FPGA ecosystem," Palmer says.

A new approach to debug

For Palmer, Certus fundamentally changes the way he approaches debug. Whereas in the past he would need to carefully think through signal access and potential problem areas early in the design process, having Certus available means there is one less thing to worry about.

"Say I have a design, and I know that modules A, B, and C are pretty good, but there are some bugs in modules D and E. Since I don't know what they are, I should instrument all of it. It doesn't matter if it's 10,000 signals – Certus takes care of it. There's enough space in the FPGA to fit that much and you don't worry about how you are going to debug it until you get it running in hardware."

Having the ability to instrument a large number of signals brings significant value when it comes to incorporating blocks of IP code as well. Over the past 5-10 years the amount of third-party IP in ASIC designs has skyrocketed. The challenge is that IP blocks are often poorly documented and off limits, and changing even a single line of code externally is very risky. Pinpointing the root cause of problems is complex, requiring access to all the signals coming from the IP.

Palmer continues, "Suppose it's a piece of processor IP, and you can't simulate enough instructions in that processor IP to figure out where the problem is occurring. A general IP block is going to be way too big for ChipScope or SignalTap to capture enough signals to be useful. The Certus tool lets me look inside someone else's IP and figure out how to debug the problems."

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Full RTL-level visibility drives productivity gains

Palmer and his team recently turned to Certus to help with debug of a high-performance computing project involving FPGA-based algorithmic acceleration. This relatively large design used 300,000 flip-flops and ran at 200 MHz. Each run through the Xilinx tools to build the chip required three to four hours of processing time.

“With ChipScope you get to look at 256 signals, which was problematic in this case because we were looking at 128-bit DRAM data buses. So 256 bits doesn't go very far,” says Palmer. “Putting Certus into the design to take advantage of the gates we didn’t use for the algorithm proved to be extremely useful. In this case we probed about 5,500 signals just because we didn’t know exactly where in the design the problems were occurring.”

The processing for this particular algorithm involved five different stages that performed different operations. When the result was different than expected, it was time to start looking for the problem areas. With Certus it was possible to quickly take a look at each processing stage. Certus ended up making the debug orders of magnitude faster.

“Being able to do one build and probe the output of each of the five stages and some of the internal pieces of the five stages reduced our iterations through place and route from 30 or so down to three,” Palmer says.

The use of Certus also boosts productivity at the Dini Group in other ways. One is support for scripts that increase workflow automation. Since Certus is completely scriptable, the Dini Group uses the GUI to generate a list, put it in a script and let a Linux machine build the entire design. Moreover, the ability to use batch mode ties into the overall flow.

Another productivity enhancer is the easy access to the full set of Certus analysis tools without the need for special connectors or hardware. By reusing the same JTAG cable used to program the FPGA, it is simple and easy to start debug right on at an FPGA workstation, without leaving the desk.

> *“To instrument 1,000 signals by hand is going to take you a few days. The Certus tool takes that few days down to a few minutes.”*
>
> Neal Palmer
> Chief Technology Officer, Dini Group

Versatility and support

Given the diverse range of projects and FPGA families covered by the Dini Group, the non-intrusive nature of the RTL based instruments and versatility of Certus has proven to be a significant benefit, particularly when coupled with knowledgeable support engineers. For instance, Palmer wanted to use Certus with new Xilinx parts that at the time were not officially supported in Certus, which in turn led to the need for a support call.

“It took me about three minutes on the phone to describe what was happening and it took about five minutes to find the information and put it in there,” recalls Palmer. “In about 10 minutes I was up and running with a new FPGA Tektronix had never seen before and it just worked. I was shocked."

Conditional captures

For many debug efforts, long capture cycles may be useful to catch intermittent areas or to simulate problems that occur over time. In these cases the Dini Group takes advantage of the conditional capture feature in Certus for in depth analysis, such as for an Ethernet application with periods of low activity.

“Being able to do conditional captures meant that instead of capturing a single packet, we could capture 10-15 packets and see what happened as time goes on through the FPGA. It made it much more useful," Palmer says, adding that another use for condition capture is watching the input to a FIFO. “If I only care about the data going into the FIFO, the conditional capture works really well for giving me only the interesting data."

Multiple clock domains

With the trend toward SoCs (System on a Chip) and embedded processors, the Dini Group and its customers increasingly need the various parts in a system to work smoothly with each other even across asynchronous clock domains. To support this requirement, Certus provides the ability to set triggers and to time correlate data across the entire system.

Brian Poladian, an engineer for the Dini Group, turned to Certus for cross-domain analysis when it came time to sort out issues in a memory controller. "In this case, we had a memory controller that runs at one rate and then internal logic that runs at another. We debugged the memory controller on one of the boards and then looked for inconsistencies in the read and write data paths across multiple clock domains. This allowed us to see when an error occurred in either the read or the write data path," he says.

Put it all together, and a major benefit of Certus for the Dini Group has been that it saves time, lots of time. It’s possible that with enough time and determination, enterprising engineers could figure out how to gain signal access in their FPGA designs and correlate signals using traditional tools.

“You could do it by yourself,” Palmer suggests, “but the problem is whenever an engineer looks at doing those things, they just give up. It's too much pain. To instrument 1,000 signals by hand is going to take you a few days. The Certus tool takes that few days down to a few minutes.”

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